AMENDMENTS TO THE CLAIMS

Please amend claims 2, 4-5, 7-9, and 11-23 as set forth below. Claims 3, 6, and 10 remain unchanged.

Claim 1 (cancelled)

2. (currently amended) A method for creating a derivative circuit design, the method comprising:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprising collecting data on a designer's available experiences and acceptable degree of risk;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification analysis on the derivative circuit design.

D1

3. (previously amended) The method of claim 2, wherein the chip layout does not exceed bounds dictated by the front-end acceptance testing.

4. (currently amended) The method of claim 2, further comprising ~~the step of~~ performing clocking and timing analysis prior to ~~the step of~~ performing verification analysis on the derivative circuit design.

5. (currently amended) The method of claim 2, further comprising ~~the step of~~ performing power analysis prior to ~~the step of~~ performing verification analysis on the derivative circuit design.

6. (previously amended) The method of claim 2, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

7. (currently amended) The method of claim 2, ~~wherein step~~ in which (a) through ~~step~~ (e) are repeated to create a second derivative circuit design, ~~such that~~ wherein a derivative circuit design is used in place of the original circuit design ~~comprises a derivative circuit design~~.

8. (currently amended) The method of claim 2, wherein ~~the step of~~ planning the chip layout comprises analyzing timing requirements to ensure the derivative circuit design meets all applicable timing requirements.

9. (currently amended) The method of claim 2, further comprising ~~the step of~~ assembling a chip based on the chip layout prior to ~~the step of~~ performing verification analysis on the derivative circuit design.

10. (previously added) The method of claim 2, wherein the original circuit design further comprises one or more non-programmable fabrics.

D' contd

11. (currently amended) The method of claim ~~10~~ 2, wherein each of the one or more programmable fabrics has a port access and hierarchical routing.

12. (currently amended) The method of claim 10, further comprising ~~the step of~~ determining a power level for each programmable fabric and each non-programmable fabric through simulation.

13. (currently amended) A computer program product that includes a computer readable medium, the computer readable medium having stored thereon a sequence of ~~carrying one or more sequences of one or more~~ instructions which, when executed by a processor, causes the processor to execute a process for creating a derivative circuit design, ~~wherein the execution of the one or more sequences of the one or more instructions causes the one or more processors to perform the steps of~~ the process comprising:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprising collecting data on a designer's available experiences and acceptable degree of risk;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification analysis on the derivative circuit design.

14. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein the chip layout does not exceed bounds dictated by the front-end acceptance testing.

15. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein the process further comprises ~~comprising the step of~~ performing clocking and timing analysis prior to ~~the step of~~ performing verification analysis on the derivative circuit design.

16. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein the process further comprises ~~comprising the step of~~ performing power analysis prior to ~~the step of~~ performing verification analysis on the derivative circuit design.

17. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

18. (currently amended) The computer ~~readable medium~~ program product of claim 13, ~~wherein step~~ in which (a) through ~~step~~ (e) are repeated to create a second derivative circuit design, ~~such that~~ wherein a derivative circuit design is used in place of the original circuit design ~~comprises a derivative circuit design~~.

19. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein ~~the step of~~ planning the chip layout comprises analyzing timing requirements to ensure the derivative circuit design meets all applicable timing requirements.

20. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein the process further comprises ~~comprising the step of~~ assembling a chip based on the chip layout prior to ~~the step of~~ performing verification analysis on the derivative circuit design.

21. (currently amended) The computer ~~readable medium~~ program product of claim 13, wherein the original circuit design further comprises one or more non-programmable fabrics.

22. (currently amended) The computer ~~readable medium~~ program product of claim ~~21~~ 13, wherein each of the one or more programmable fabrics has a port access and hierarchical routing.

D1 cont'd

23. (currently amended) The computer ~~readable medium~~ program product of claim 21, wherein the process further ~~comprising~~ comprises ~~the step of~~ determining a power level for each programmable fabric and each non-programmable fabric through simulation.